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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,240	06/26/2003	Yasuhiko Tsukikawa	67161-047	4239

7590 10/08/2004

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,240	TSUKIKAWA ET AL.	
	Examiner	Art Unit	
	Thong Q. Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13 and 16* is/are allowed.

6)☒ Claim(s) *1-3,12,14 and 15* is/are rejected.

7)☒ Claim(s) *4-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on September 21, 2004 has been entered.

2. Claims 1-16 are presented for examination.

Response to Arguments

3. Applicant's arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1-3, 12, 14-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Arimoto et al. (U.S. Patent No. 6,573,613).

Regarding claims1, 12, Arimoto et al. disclose a semiconductor memory device (Figure 3) comprising:

a plurality of memory cells arranged in rows and columns (Figure 3),

said plurality of memory cells (Figure 4) being divided into a plurality of storage units each formed of the two memory cells (Mca, MCb) bearing complementary data;

a plurality of bit lines (/Bla, Bla) forming pairs each including the two bit lines and arranged corresponding to the columns of said memory cells, respectively;

a plurality of word lines (WL) arranged corresponding to the rows of said memory cells, respectively, and extending in a direction crossing said plurality of bit lines (Column 2, lines 65-67, Column 3 lines 1-18); and

a plurality of cell plates (Figure 4, Cpa) provided corresponding to said storage units, respectively, and each isolated at least electrically from the others, wherein

each of said plurality of memory cells (Figure 4, Mca) includes:

a select transistor (ATRa) connected between the corresponding bit line (Bla) and a storage node (Figure 4) , and being turned on or off in accordance with a voltage on the corresponding word line (Column 3, lines 1-18) , and

a capacitor (Figure 4, Sca) connected between said storage node and the corresponding cell plate (Figure 4).

Regarding claims 2-3, 14-15, Arimoto et al. disclose wherein gates of the select transistors in said two memory cells forming the same storage unit are connected to the word lines different from each other, respectively (Figure 4, Wla, WLb), and wherein each of said plurality of memory cells further includes an active region extending in an

extending direction of the corresponding bit line and defining a formation region of said select transistor, said active region extends continuously through a portion between the two memory cells neighboring to each other in the extending direction of the corresponding bit line, and said semiconductor memory device further comprises: a bit line contact provided for each of sets each including the neighboring two memory cells, and electrically connecting the corresponding active region to the corresponding bit line (Column 3, lines 1-18, Figures 5-6).

Allowable Subject Matter

6. Claims 4-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 4-11 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Arimoto et al. (U.S. Patent No. 6,573,613), and others, does not teach the claimed invention having a gates of the select transistors in the two of memory cells forming the same storage unit are connected to the same word line.

7. Claims 13, 16 are allowed.

Claims 13, 16 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Arimoto et al. (U.S. Patent No. 6,573,613), and others, does not teach the claimed invention having a select transistor connected between the other of

paired two bit lines and the cell plate without interposing a capacitor, and being turned on or off in accordance with the voltage on the corresponding word line.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2818

THONG LE
PRIMARY EXAMINER